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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,775	03/15/2004	Isao Shimizu		8630

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,775	SHIMIZU ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/692,468.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/15/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Action in response to the instant U.S. Application 10/799,775, US 20040175850A1, filed March 15, 2004, which is CON of 10/140,043 05/08/2002 PAT 6,727,723, which is a DIV of 09/692,468 filed 10/20/2000 PAT 6,400,173.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), for JP 11-329281, filed 11/19/1999. The certified copy has been filed in parent Application No. 09/692,468 filed on 10/20/2000.

Claims 25-40 are presently pending and under examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 25-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 25, 32, 33, 39, 40, recite the phrase "in such a manner", which renders the claims indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. The phrase "in such a manner" fails to positively describe the step of superimposing the probe substrate on the semiconductor in relation to the conductive needles. See MPEP § 2173.05(d).

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 25-32, 39 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7 of Shimizu et al. (U.S. Patent No. 6,727,723). Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed invention of the instant Application includes the claimed limitations recited in the reference U.S. Patent.

Claims 1-7 of the U.S. Patent contains every element of claims 25-32, 39 of the instant application and as such anticipates claims 25-32, 39 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting

because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claims 33-38, 40 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7 of Shimizu et al. (U.S. Patent No. 6,727,723) in view of Tada et al. (U.S. Patent No. 4,799,009).

Regarding Claims 33, 40, Shimizu does not recite, "forming a plurality of second semiconductor circuits each having a desired function different from the desired function of the plurality of first semiconductor circuits on a second semiconductor wafer and each corresponding to a second semiconductor chip as a second product". However, Tada discloses a wafer testing-device in which a plurality of wafers can be tested simultaneously significantly reducing the time required for testing each chip, where a prober is provided which receives a wafer to be tested. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to test multiple wafers in the patent of Shimizu as taught by Tada, since testing a plurality of wafers simultaneously significantly reducing the time required for testing each chip.

Regarding Claims 34-38, Shimizu et al. (U.S. Patent No. 6,727,723) recite Claims 4-7, which contain every element of claims 34-38 of the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 25-32, 39 are rejected under 35 U.S.C. 102(b) as being anticipated by Kwon et al. (U.S. Patent No. 5,070,297).

Regarding independent Claims 25, 32, 39, Kwon discloses a method for a full wafer integrated circuit testing device, (Figures 2 and 3), comprising:

Forming a plurality of semiconductor chips (15) as a wafer each having a function, as disclosed in the abstract.

Placing a test circuit wafer probe card 10 in conjunction with a test control unit 40 (Figure 1), the probe card comprising a probe unit die matrix 12 that comprises a plurality of individual probe units 14 connected to conductive needles probe tips (16) and operated in accordance with a program of the test control unit (40) to test the wafer semiconductor chips (15), where the wafer probe card is on a probe silicon substrate 38 with a size corresponding to the wafer semiconductor chips (15), and having the conductive needles 16 formed in alignment with the placement of electrode pads 19 on

the wafer semiconductor chips 15, as shown in (Figure 2). Programmable logic ICs individual probe units 14 including logic such as comparators (54 and 56) provided on the probe substrate 38 of card 10 in association with respective wafer semiconductor chips 15, where each semiconductor chip 15 is tested by the corresponding test circuit probe units 14 and where each probe unit 14 engages each integrated circuit chip 15, as show in (Figures 2 and 3).

Superimposing the probe substrate 38 of card 10 on the wafer semiconductor chip (15), where that the needles 16 are brought into contact with the corresponding electrode pads 19 of the semiconductor chips 15 as shown in (Figure 2) where the probe unit 14 engages the integrated circuit chips 15, so that pointed tip 18 engages integrated circuit chip pad 19.

Testing each semiconductor chip 15 by the test circuit 14, where the test control unit 40 engages probe card 10, which connects to integrated circuit chips such as 42 and 44 via probe tips 16, (Figure 3).

Selecting a semiconductor chip15 judged to be non-defective, as a product according to the test. Comparators 54 and 56 compare the expected output bus 82 to the actual signals from signal repeaters 50 and 52 to determine if the signals match, thus indicating a fully functional integrated circuit. If no match occurs, however, the comparator 54 or 56 (or both) will send a fail signal to fail condition register 66 or 68, as appropriate. Fail condition registers 66 and 68 each has a memory for temporarily storing these signals from the comparator 54 and 56, respectively.

Regarding Claim 26, Kwon discloses programmable logic ICs individual probe units 14 comprising logic such as comparators (54 and 56) provided on the probe substrate 38 of card 10 in association with respective wafer semiconductor chips 15, where each semiconductor chip 15 is tested by the corresponding test circuit probe units 14 and where each probe unit 14 engages each integrated circuit chip 15, as show in (Figures 2 and 3).

Regarding Claims 27, 28, 30, Kwon discloses a test circuit probe card 10, which generates test signals to each semiconductor chip 42 and 44 via probe tips 16 through signal repeaters such as 46 and 48 connected to the input signal bus 78. The input signals are tested based on the output test signals fro repeaters 50 and 52, in accordance with a predetermined algorithm, such as expected values on the output bus 82, (Figure 3).

Regarding Claim 29, Kwon discloses probe card 10 in conjunction with a test control unit 40 including memory, which inherently is part of every computerized control unit which stores a program, which generates control signals for test signal buses that lead from test control unit 40 to probe card 10 including input signal bus 78, address bus 80, expected output bus 82, and fail code bus 84, (Figure 3).

Regarding Claims 31, Kwon discloses memory control unit 40, which is a rewritable memory because it reads and writes continuous test dada from memory components (66 and 68), which store data associated with signals from test control unit (40) and the integrated circuit (15), (Figure 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 33-38, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (U.S. Patent No. 5,070,297) in view of Tada et al. (U.S. Patent No. 4,799,009).

Regarding Claims 33, 40, Kwon does not recite, "forming a plurality of second semiconductor circuits each having a desired function different from the desired function of the plurality of first semiconductor circuits on a second semiconductor wafer and each corresponding to a second semiconductor chip as a second product". However, Tada discloses a wafer testing-device in which a plurality of wafers can be tested simultaneously significantly reducing the time required for testing each chip, where a prober is provided which receives a wafer to be tested. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to test multiple wafers in the patent of Shimizu as taught by Tada, since testing a plurality of wafers simultaneously significantly reducing the time required for testing each chip.

Regarding Claims 34, 35, 37, Kwon discloses a test circuit probe card 10, which generates test signals to each semiconductor chip 42 and 44 via probe tips 16 through signal repeaters such as 46 and 48 connected to the input signal bus 78. The input signals are tested based on the output test signals fro repeaters 50 and 52, in accordance with a predetermined algorithm, such as expected values on the output bus 82, (Figure 3).

Regarding Claim 36, Kwon discloses probe card 10 in conjunction with a test control unit 40 including memory, which inherently is part of every computerized control unit which stores a program, which generates control signals for test signal buses that lead from test control unit 40 to probe card 10 including input signal bus 78, address bus 80, expected output bus 82, and fail code bus 84, (Figure 3).

Regarding Claims 38, Kwon discloses memory control unit 40, which is a rewritable memory because it reads and writes continuous test dada from memory components (66 and 68), which store data associated with signals from test control unit (40) and the integrated circuit (15), (Figure 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2138

By: _____

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